PCT/GB 98 / 01734
09/446008

The Patent Office

The Patent Office
Concept House
Cardiff Road
Newport
South Wales
NP9 1RH

REC'D 30 JUL 1998
WIPO PCT

PRIORITY DOCUMENT

SUBMITTED OR TRANSMITTED IN COMPLIANCE WITH RULE 17.1(a) OR (b)

I, the undersigned, being an officer duly authorised in accordance with Section 74(1) and (4) of the Deregulation & Contracting Out Act 1994, to sign and issue certificates on behalf of the Comptroller-General, hereby certify that annexed hereto is a true copy of the documents as originally filed in connection with the patent application identified therein.

In accordance with the Patents (Companies Re-registration) Rules 1982, if a company named in this certificate and any accompanying documents has re-registered under the Companies Act 1980 with the same name as that with which it was registered immediately before re-registration save for the substitution as, or inclusion as, the last part of the name of the words "public limited company" or their equivalents in Welsh, references to the name of the company in this certificate and any accompanying documents shall be treated as references to the name with which it is so re-registered.

In accordance with the rules, the words "public limited company" may be replaced by p.l.c., plc, P.L.C. or PLC.

Re-registration under the Companies Act does not constitute a new legal entity but merely subjects the company to certain additional company law rules.

Signed

Dated 15 JUL 1998

Patents Form 1/77

Patent[redacted]77
(Rule [redacted])

The Patent Office

FEE COPY 1/77

THE PATENT OFFICE
A
16 JUN 1997
RECEIVED BY FAX

Request for grant of a patent

(See the notes on the back of this form. You can also get an explanatory leaflet from the Patent Office to help you fill in this form)

The Patent Office

Cardiff Road
Newport
Gwent NP9 1RH

9712368.1

1. Your reference — DERA/HO/COM/IPD65/P2567

2. Patent application number *(The Patent Office will fill in this part)* — 16 JUN 1997

16JUN97 E281863-1 D02776
P01/7700 25.00 - 9712368.1

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

The Secretary of State for Defence
Defence Evaluation and Research Agency
DERA Farnborough
Farnborough, Hants. GU14 0LX

[redacted]

Patents ADP number *(if you know it)*

If the applicant is a corporate body, give the country/state of its incorporation — United Kingdom

6997670008

4. Title of the invention — Photodetector Circuit

5. Name of your agent *(if you have one)* — A.O.Bowdery *et al.*

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

Formalities Section (DERA)
Directorate of Intellectual Property Rights
MOD (PE) Abbey Wood #19
PO Box 702
Bristol
BS12 7DU

6997910003

[redacted]

Patents ADP number *(if you know it)* — 2576002

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number

Country	Piority application number *(if you know it)*	Date of filing *(day / month / year)*

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number or earlier application	Date of filing *(day / month / year)*

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:*

a) any applicant named in part 3 is not an inventor, or
b) there is an inventor who is not named as an applicant, or
c) any named applicant is a corporate body.
See note (d))

Yes

THE PATENT OFFICE
A
16 JUN 1997
RECEIVED BY FAX

Patents Form 1/77

9. Enter the number of sheets for any of the following items you are filing with this form. Do not count copies of the same document

Continuation sheets of this form	
Description	8 ✓
Claim(s)	4 ✓
Abstract	1 ✓
Drawing(s)	1 ✓

SMB

10. If you are also filing any of the following, state how many against each item.

Priority documents	
Translations of priority documents	
Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	1
Request for preliminary examination and search *(Patents Form 9/77)*	1
Request for substantive examination *(Patents Form 10/77)*	
Any other documents *(please specify)*	

11. I / We request the grant of a patent on the basis of this application.

Signature A.W.S.Williams Date 16 June 1997

12. Name and daytime telephone number of person to contact in the United Kingdom A.W.S.Williams Tel.: (01684) 894122

Warning

After an application for a patent has been filed, the Comptroller of the Patent Office will consider whether publication or communication of the invention should be prohibited or restricted under Section 22 of the Patents Act 1977. You will be informed if it is necessary to prohibit or restrict your invention in this way. Furthermore, if you live in the United Kingdom, Section 23 of the Patents Act 1977 stops you from applying for a patent abroad without first getting written permission from the Patent Office unless an application has been filed at least 6 weeks beforehand in the United Kingdom for a patent of the same invention and either no direction prohibiting publication or communication has been given, or any such direction has been revoked.

Notes

a) *If you need help to fill in this form or have any questions, please contact the Patent Office on 0645 500505.*

b) *Write your answers in capital letters using black ink or you may type them.*

c) *If there is not enough space for all the relevant details on any part of this form, please continue on a separate sheet of paper and write "see continuation sheet" in the relevant part(s). Any continuation sheet should be attached to this form.*

d) *If you have attached 'Yes' Patents Form 7/77 will need to be filed.*

e) *Once you have filled in the form you must remember to sign and date it.*

For details of the fee and ways to pay please contact the Patent Office.

DUPLICATE

PATENT SPECIFICATION

TITLE: PHOTODETECTOR CIRCUIT

APPLICANT: The Secretary of State for Defence

INVENTORS: Gillian Fiona MARSHALL

Stephen COLLINS

DERA Malvern
St Andrews Road
Malvern
Worcs.
WR14 3PS

AGENT'S REFERENCE: DERA/HO/COM/IPD65/P2567

COUNTRY: United Kingdom

DUPLICATE

PHOTODETECTOR CIRCUIT

This invention relates to a photodetector circuit.

Semiconductor photodetectors based on the silicon bandgap are suitable for operation in the visible and near infrared region of the spectrum. Prior art silicon photodetectors can be constructed in compact form and cheaply using mature CMOS technology. Photon illumination of a photodiode results in the generation of an electrical current, the photocurrent. It is desirable for many applications for the photodetector to be responsive to a very wide range of input intensities. This is facilitated by passing the photocurrent through a MOSFET load device operating in its subthreshold regime. In this regime, MOSFET output (voltage) response is a logarithmic function of its input (current). Thus the combined photodiode/MOSFET device has a logarithmic illumination versus output voltage characteristic. The dynamic range of the overall system is very large: detectable illumination may vary by as much as 5 or 6 orders of magnitude.

A problem with such prior art devices is that the MOSFETs have inherent leakage currents which represent a substantially constant loss in a stable environment. Leakage current is not a significant problem in high illumination intensity when the MOSFET is operated at current levels far larger than the leakage level. However, it can severely degrade detector sensitivity at low light levels when photocurrent may potentially be even smaller than leakage current. Very low light sensitivity has been improved by moving from pure CMOS to parasitic bipolar circuitry within a CMOS process. While this may have some specialist applications, the cheaper and more compact pure CMOS devices work acceptably well down to twilight illumination levels and the adaptation is not generally worthwhile.

A more fundamental obstacle to the general portability of CMOS photodetectors is their temperature instability. Leakage currents are highly temperature dependent and increase severely at elevated temperatures. This is potentially a serious barrier to the commercial uptake of CMOS detectors in instruments such as the recently developed digital cameras. This is despite the inherent cost and performance advantage offered by CMOS over currently used CCD detectors. There is a

perceived market for a single camera which operates effectively in the variety of environments and throughout the whole range of illumination levels to be anticipated by the modern photographer.

The low-light sensitivity of pure CMOS photodetectors has been improved by operating at low temperatures and exploiting the consequent reduction in leakage current. However cooling apparatus e.g. Peltier cooler or dewar, is bulky and represents a significant drain on power sources, proving inconvenient to numerous applications.

It is the object of this invention to provide a photodetector with improved temperature stability.

The present invention provides a photodetector circuit incorporating photon detecting means arranged to produce an electric current in response to incident photon illumination associated with a current load device arranged to produce a voltage response to current flow characterised in that

(a) the photon detecting means is arranged to provide an output current which is supplied to the current load device,

(b) the current load device has a current-voltage characteristic in which the voltage is a logarithmic function of current flow, and

(c) the photon detecting means is a phototransistor with a current gain factor greater than unity.

This invention provides the advantage of improved temperature stability compared to prior art photodetecting devices which are also capable of responding to a large dynamic range of incident illumination intensities. The gain of the phototransistor acts on the generated photocurrent to produce an output current larger by a factor of ~ 100 in comparison with that generated by a comparable *p-n* photodiode. This amplification of the current supplied to the current load device ensures that current within the load is generally much higher than the leakage current, even at elevated temperatures and yet still maintains the load logarithmic voltage response. Leakage current therefore represents only a small loss from the perceived photocurrent and accurate intensity measurements can be made at low illumination levels.

In order that the invention might be more fully understood, an embodiment thereof will now be described with reference to the accompanying drawings in which:

Figure 1 is a circuit diagram of a prior art photodetector pixel.

Figure 2 is circuit diagram of a photodetector pixel of the invention.

With reference to *Figure 1*, a pixel of a prior art photodetector circuit is illustrated generally by 10. This photodetector pixel 10 is suitable for incorporation in an array of like pixels to create a detector array. The photodetector pixel 10 comprises a photodiode 12 and load metal oxide field effect transistor (MOSFET) 14 connected via MOSFET source 16 at connection node 18. The MOSFET 14 also has drain connected to both gate and power supply V_{DD} and therefore constitutes a load for the photodiode 12. In this arrangement light 20 incident on the photodiode 12 results in a photocurrent I_{ph} and voltage V_{ph} being developed at the connection 18. This connection 18 is buffered from a constant current sink (not shown) by a second MOSFET 22. The second MOSFET 22 has gate 24 connected to the connection 18, drain 26 connected to the power supply V_{DD} and source 28 to a MOSFET switch 30. It thus constitutes a source-follower driver. A switch voltage (V_{sw}) may be applied to a MOSFET gate 32 in order to operate the MOSFET switch 30. This provides for an output voltage (V_{out}) to develop at a pixel output line 34 which is connected to an array readout circuit (not shown).

Figure 2 illustrates a photodetector pixel circuit of the invention, indicated generally by 100. This photodetector pixel 100 comprises a number of components which are common to the prior art device 10. Such components are referenced by numbers 100 greater than the corresponding references in *Figure 1* and include: a load MOSFET 114 with source 116 connected to connection node 118 and drain and gate connected as for *Figure 1*; second MOSFET 122 with gate 124, drain 126 and source 128 connected as for *Figure 1*; switching MOSFET 130 addressed via its gate 132; and pixel output line 134. The photodetector pixel of the invention 100 also includes a bipolar phototransistor 200. The bipolar phototransistor 200 has its emitter connected to connection node 118.

With reference to *Figure 1*, the operation of the prior art photodetector pixel 10 will now be described. Light 20 incident on the photodiode 12 results in the generation of photocurrent I_{ph}. This current is constrained to flow as the source-drain current of the load MOSFET 14 by virtue of its isolation from the remainder of the circuit by the second MOSFET 22. A fraction of this photocurrent is however lost from the MOSFET 14 as a leakage current $I_{leakage}$, and the MOSFET 14 actually operates at an input channel current I_{ch}. In consequence of this channel current I_{ch}, a voltage difference (V_{gs}) develops between gate and source of the load MOSFET 14 to the extent necessary to operate the load MOSFET 14 at this current I_{ch}. This voltage difference V_{gs} is attained by driving a voltage at the MOSFET source 16 to a value V_{ph} ($\cong V_{DD} - V_{gs}$). This voltage V_{ph} is therefore that appearing on the connection node 18, which contains information regarding illumination intensity and which is consequently termed the photovoltage. The photodetector 12 is constructed such that over a range of expected illumination intensities, the generated photocurrent (I_{ph}) is much less than that needed to drive the voltage difference V_{gs} above the load MOSFET threshold voltage. The MOSFET 14 therefore operates in its subthreshold regime. In this regime, a MOSFET drain current (I_d) is an exponential function of its gate-source voltage difference (V_{gs}) and therefore also of its source voltage (V_s): $I_d \propto \exp(V_s)$. In the photodetector circuit 10, the gate voltage is held at V_{DD} and the source voltage is the photovoltage V_{ph} developed at connection 18. The drain current is the channel current I_{ch}, and so:

$$I_{ch} \propto \exp(V_{ph})$$

$$\Rightarrow V_{ph} \propto \ln I_{ch}$$

$$\text{and } V_{ph} \propto \ln(I_{ph} - I_{leakage})$$

Thus, if the leakage current is negligible in comparison with the generated photocurrent, the photovoltage is proportional to the logarithm of the photocurrent response: $V_{ph} \propto \ln I_{ph}$.

The voltage V_{ph} generated at connection 18 is applied to the gate 24 of the second MOSFET 22. The drain-source current of this MOSFET 22 is constant, constrained by the constant current sink. The voltage (V_{sf}) at the source 28 of this MOSFET 22 therefore follows any variation in the gate voltage (photovoltage V_{ph}) in order to maintain this constant current. The MOSFET 22 thus functions as a source-follower

driver: $V_{sf} = V_{ph} - \Delta$, where Δ is the voltage drop required to operate the MOSFET at the current provided by the constant current sink. This MOSFET 22 isolates the connection node 18 and therefore provides a buffering capability between the connection node 18 and readout circuit. The voltage (V_{ph}) at connection 18 is thus free to vary in accordance with the photocurrent (I_{ph}) with negligible influence from the readout circuit. In summary, the MOSFET 22 drives its source voltage V_{sf} to follow the photovoltage V_{ph}, a logarithmic function of the photocurrent I_{ph}.

Switching MOSFET 30 acts to switch a voltage on the source 28 of the second MOSFET 22 to the pixel output line 34, the output line 34 being shared by several pixels. Application of an appropriate voltage (V_{sw}) to the gate 32 turns the switching MOSFET 30 ON and whatever voltage is present on the source 28 of the second MOSFET 22 is passed substantially unaffected to the pixel output line 34 as output voltage V_{out}. In this way, a pixel is addressed via a voltage (V_{sw}) to the switching MOSFET 30 which enables the output voltage (V_{out}) to be read by the readout circuit. This output voltage (V_{out}) is a measure of the photovoltage (V_{ph}) developed at the load MOSFET source 16 in response to illumination of the photodiode 12. In particular:

$$V_{out} \cong V_{sf} = V_{ph} - \Delta, \text{ and}$$

$$V_{ph} \propto \ln (I_{ph} - I_{leakage})$$

In situations in which the leakage current is negligible, the prior art photodetector pixel 10 thus produces an addressable output voltage which is a measure of the logarithm of the input illumination intensity.

If the leakage current is not negligible the prior art photodetector sensitivity is reduced. In some working environments e.g. an air-conditioned office, the temperature is generally sufficiently stable and cool and the illumination intensity adequately high that no significant reduction in sensitivity occurs. However, at higher temperatures leakage current increases dramatically and picture quality in darker areas of even a standard scene may be severely degraded. Thus prior art CMOS imagers are not appropriate if required to be used in differing environments or in those for which a variety of ambient temperatures are anticipated.

With reference to *Figure 2*, the operation of the photodetector pixel of the invention will now be described. The bipolar phototransistor 200 provides an output current I_{bi} which is a measure of incident light 120 intensity. Bipolar phototransistors are known in the prior art. They behave essentially as standard bipolar transistors but the base signal is generated by photon illumination. The base current is similar in magnitude to that of a photodiode fabricated from identical materials. The collector current is equal to the base current multiplied by the transistor gain factor β. A typical phototransistor structure has a β value of around 100. Thus, in this invention, the current output from the phototransistor 200 is given by

$$I_{bi} \cong \beta\, I'_{ph}$$

where I'_{ph} is the current which is generated by a photodiode fabricated from the same base-emitter material.

Illumination of phototransistor 200 therefore results in the generation of a bipolar photocurrent I_{bi}. Thereafter, operation of many components of *Figure 2* are similar to those of *Figure 1*. Voltages generated which are analogous to those within the prior art photodetector pixel 10 but dependent on bipolar current I_{bi} as opposed to I_{ph} will be indicated as such by the use of the previous symbol primed. The bipolar photocurrent I_{bi} is constrained to flow as the source-drain current of the load MOSFET 114. The gate-source voltage of the MOSFET 114 is raised to a level consistent with the actual channel current: the bipolar photocurrent I_{bi} less an amount lost as MOSFET leakage current $I'_{leakage}$, which causes a voltage V'_{ph} to develop at connection node 118. The bipolar photocurrent operates the MOSFET 114 in its subthreshold regime and so $V'_{ph} \propto \ln (I_{bi} - I'_{leakage})$. The second MOSFET 122 is configured as a source-follower driver and so V'_{ph} is passed from its gate connection with connection 118 to source 128, less an offset Δ'. This source voltage is passed to the pixel output line 134 as V'_{out} on activation of the switching MOSFET 130. Thus the photodetector pixel 100 of the invention provides an addressable output voltage which is given by

$$V'_{out} \cong V'_{ph} - \Delta', \text{ and}$$

$$V'_{ph} \propto \ln (I_{bi} - I'_{leakage}),$$

and which is therefore a measure of the logarithm of the input illumination intensity. In this invention however, the phototransistor current is a factor of ~ 100 larger than the equivalent photodiode current generated in the prior art device:

$$V'_{ph} \propto \ln(\beta I'_{ph} - I'_{leakage}),\ \beta \sim 100$$

In both photodetector pixel circuits 10, 100 herein described, the leakage current occurs at the load MOSFET 14, 114. This leakage is a significant proportion of the photocurrent if the photocurrent is at the low end of its range i.e. low illumination and/or high operating temperature. By using a phototransistor in place of a conventional photodiode the photocurrent is magnified by a gain factor β which appears to the pixel circuit to be equivalent to an increased photocurrent. This larger current through the load MOSFET 114 effectively raises the operating regime of the load MOSFET 114 above problematic leakage levels. Variations in the leakage current $I'_{leakage}$ due to temperature fluctuations will not significantly affect $\beta I'_{ph}$, despite an order of magnitude equivalence between I'_{ph} and $I'_{leakage}$.

The photodetector circuit 100 of the invention is fabricated in BiCMOS technology. BiCMOS is optimised for both bipolar and CMOS technology but it is significantly more expensive to implement than CMOS. For most applications the expense of BiCMOS cannot be justified and its adoption is not normally considered. However, the advantages to be gained in reducing the temperature sensitivity of large dynamic range photodetectors while still maintaining accurate pixel resolution justify this surprising application of BiCMOS.

It will be appreciated by one skilled in the art of circuit design that only one embodiment is described herein and the invention may be equivalently implemented in a variety of bipolar transistor - MOSFET combinations. In this embodiment a pnp phototransistor is illustrated with an NMOS load. Both pnp and npn phototransistors may be used in combination with either NMOS or PMOS loads to produce the temperature-robust photodetector of the invention. Preference for a particular combination may be for a variety of reasons - a likely consideration will be the way in which the BiCMOS fabrication process is implemented.

In another embodiment, an intensity attenuator is incorporated in the invention. This enables the photodetector 100 to function comparably with prior art devices at high illumination intensities. The attenuator is arranged to reduce the incident light intensity in high-illumination situations prior to its detection by the phototransistor. This effectively raises the illumination upper threshold at which the pixel circuit 100 can operate. This is necessary to maintain load MOSFET 114 operation in its subthreshold region. There is a maximum MOSFET current limit, above which the characteristic is no longer logarithmic and saturation begins to occur. This embodiment of the invention effectively shifts this upper limit to a higher illumination. This maintains a large operating range despite gain being included in the photodetector to counteract performance degradation in variable temperature environments. The attenuation may be provided by, for example, reducing the photodetector lens aperture.

Standard CMOS technology is most effectively used in circuit designs based on MOSFET elements. Bipolar phototransistors may be manufactured in CMOS as a parasitic lateral or vertical bipolar transistor, but this is not ideal as such devices are not optimised on a standard CMOS process. Although they may be suitable for some applications, these bipolar phototransistors are large and have low matching. The former feature forces the detector designer to accept either poor pixel spatial resolution or an expensive requirement for a physically large array. The latter feature leads to high fixed pattern noise. These disadvantages have been accepted in some applications requiring very low-light sensitivity, and they may also prove acceptable when the purpose is to provide temperature insensitivity.

However an additional advantage provided by BiCMOS still remains. BiCMOS allows the readout circuit to be made with lower noise that an equivalent CMOS circuit, thus increasing the performance of the photodetecting system still further.

CLAIMS

1. A photodetector circuit (100) incorporating photon detecting means (200) arranged to produce an electric current (I_{bi}) in response to incident photon illumination associated with a current load device (114) arranged to produce a voltage (V'_{gs}, V'_{ph}) response to current flow characterised in that
   (a) the photon detecting means (200) is arranged to provide an output current (I_{bi}) which is supplied to the current load device (114),
   (b) the current load device (114) has a current-voltage characteristic in which the voltage is a logarithmic function of current flow, and
   (c) the photon detecting means (200) is a phototransistor with a current gain factor (β) greater than unity.

2. A photodetector circuit (100) according to Claim 1 characterised in that the current load device (114) is a MOSFET device with its source (116) or drain connected to the phototransistor (200) and the phototransistor (200) is arranged to produce an electric current (I_{bi}) which is low enough to operate the MOSFET (114) in its subthreshold regime.

3. A photodetector circuit (100) according to Claim 2 characterised in that the phototransistor (200) is a bipolar transistor incorporating a photodetecting base region and with emitter connected to the load MOSFET (114).

4. A photodetector circuit (100) incorporating photon detecting means (200) arranged to produce an electric current (I_{bi}) in response to incident photon illumination associated with a current load device (114) arranged to produce a voltage (V'_{gs}, V'_{ph}) response to current flow characterised in that the photodetector (100) sensitivity is substantially unaffected by environmental temperature variations within a range -20 to 60°C wherein
   (a) the photon detecting means (200) is arranged to provide an output current (I_{bi}) which is supplied to the current load device (114),
   (b) the current load device (114) has a current-voltage characteristic in which the voltage is a logarithmic function of current flow, and
   (c) the photon detecting means (200) is a phototransistor with a current gain factor (β) greater than unity.

5. A photodetector circuit (100) according to Claim 4 characterised in that the current load device (114) is a MOSFET device with its source (116) or drain connected to the phototransistor (200) and the phototransistor (200) is arranged to produce an output current (I_{bi}) which is sufficiently low to operate the MOSFET (114) in its subthreshold regime.

6. A photodetector circuit (100) according to Claim 5 characterised in that the phototransistor (200) is a bipolar transistor incorporating a photodetecting base region and with emitter connected to the load MOSFET (114).

7. A photodetector circuit (100) according to any preceding claim characterised in that the photodetector (100) is for the purpose of operation in environmental temperatures ranging from -20 to 60°C with substantially unaffected sensitivity at illumination levels down to 1 lux.

8. A photodetector circuit (100) according to any preceding claim characterised in that the phototransistor (200) and current load device (114) are fabricated using BiCMOS technology.

9. A photodetector circuit (100) according to any preceding claim characterised in that the circuit (100) incorporates an attenuator arranged to reduce the intensity of light (120) prior to incidence on the photon detecting means (200) to an extent necessary to provide for the resultant output current (I_{bi}) to be low enough to operate the MOSFET (114) in its subthreshold regime.

10. A photodetector circuit (100) according to Claim 9 characterised in the photodetector (100) is capable of operation in environmental temperatures ranging from -20 to 60°C with substantially constant contrast sensitivity.

11. A photodetector circuit (100) according to Claim 3 or 6 characterised in that the load MOSFET (114) and phototransistor (200) are connected at a common connection point (118) to buffering means (122) and the buffering means (122) is connected to a pixel readout circuit.

12. A photodetector circuit (100) according to any preceding claim characterised in that it is incorporated in an array of like circuits (100).

13. A temperature-robust photodetector circuit (100) characterised in that it includes a bipolar phototransistor (200), a load MOSFET (114) and voltage detecting means (122, 130, 134) wherein:
    (a) the bipolar phototransistor (200) is arranged to supply photocurrent output (I_{bi}) to the load MOSFET (114),
    (b) the phototransistor (200) is arranged such that photocurrent output (I_{bi}) is sufficiently small to maintain subthreshold operation of the load MOSFET (114), and
    (c) voltage detecting means (122, 130, 134) is arranged to detect a voltage output from the load MOSFET (114) in response to photocurrent supply.

14. A temperature-robust photodetector circuit (100) characterised in that it includes a bipolar phototransistor (200), a load MOSFET (114) and voltage detecting means (122, 130, 134) wherein:
    (a) the bipolar phototransistor (200) is arranged to supply photocurrent output (I_{bi}) to the load MOSFET (114),
    (b) the phototransistor (200) is arranged such that photocurrent output (I_{bi}) is sufficiently small to maintain subthreshold operation of the load MOSFET,
    (c) voltage detecting means (122, 130, 134) is arranged to detect a voltage output from the load MOSFET (114) in response to photocurrent supply, and
    (d) the phototransistor (200) and load MOSFET (114) are fabricated using BiCMOS technology.

15. A temperature-insensitive method of measuring photon radiation intensity over a dynamic range greater than four orders of magnitude characterised in that the method comprises the steps of:
    (a) providing a BiCMOS-fabricated photodetector circuit (100) comprising a bipolar phototransistor (200) arranged to supply output current (I_{bi}) to a load MOSFET (114).

(b) arranging the phototransistor (200) to respond to incident radiation (120) by providing output current (I_{bi}) to operate the load MOSFET (114) subthreshold,

(c) detecting the load MOSFET output voltage (V_{ph}) response to said output current (I_{bi}).

16. A detector array characterised in that it is an array of photodetector circuits each in accordance with Claim 1.

17. A digital camera characterised in that it incorporates an array of photodetector circuits each in accordance with Claim 1.

ABSTRACT

A photodetector circuit (100) fabricated in BiCMOS exhibits improved temperature stability. A bipolar phototransistor (200) generates a photocurrent (I_{bi}) in response to illumination. This photocurrent (I_{bi}) is passed through a diode connected load MOSFET (114) operating subthreshold which gives a logarithmic voltage output. This ensures a large dynamic range of the photon detection system. The phototransistor (200) has gain (β) which amplifies an initial current response and ensures that current (I_{bi}) through the load MOSFET (114) is significantly higher than MOSFET leakage current. This improves performance at high temperatures when the leakage current is large, whilst maintaining photodetector sensitivity to low illumination levels.

Figure 2 should accompany this abstract.

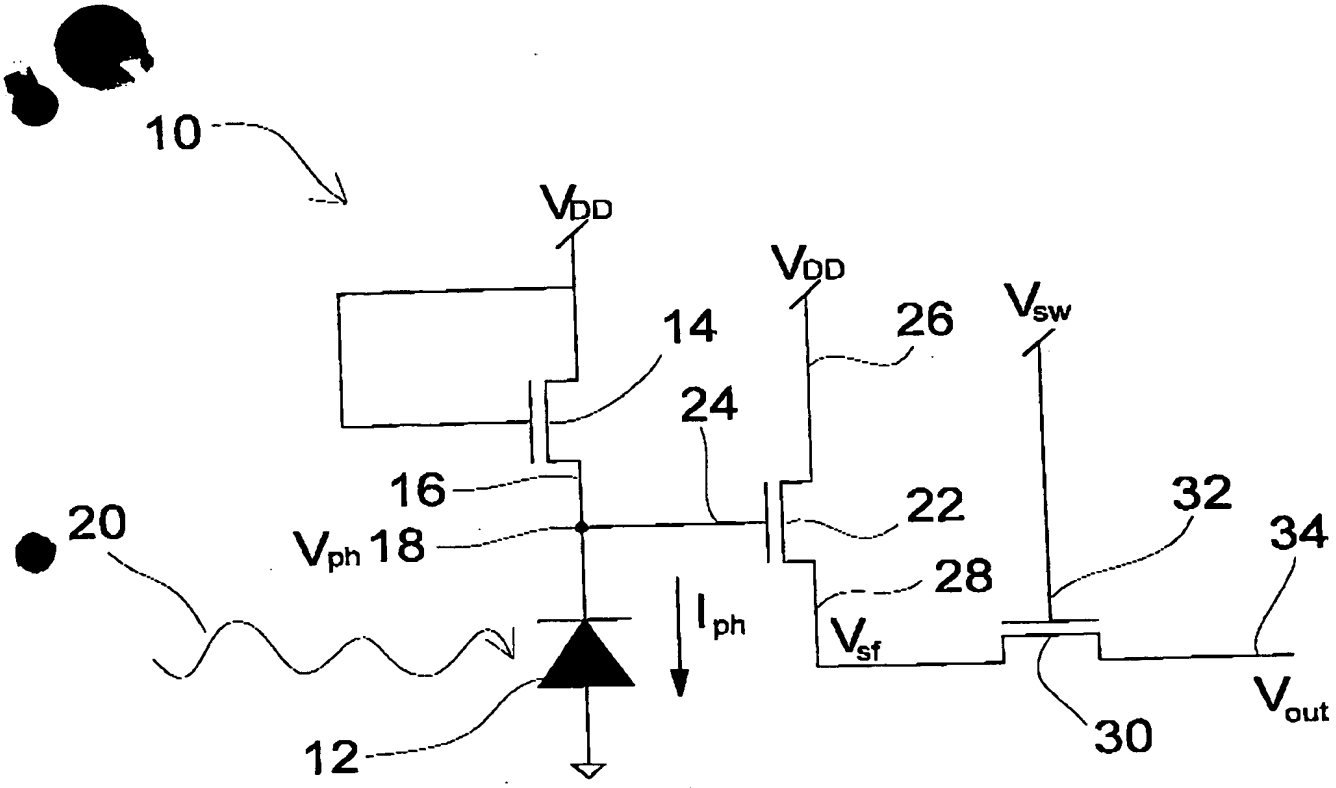

Figure 1 - Prior Art

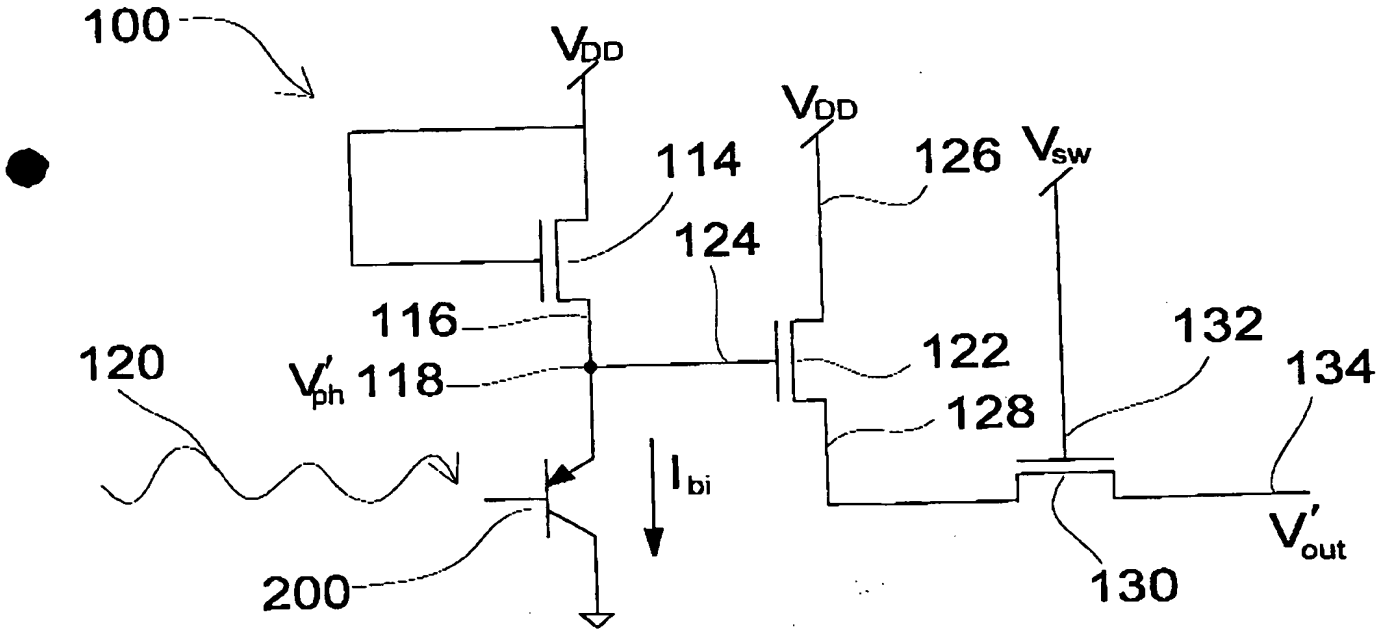

Figure 2

PCT/GB 98/01734.

D/IPR (DERA).

15.6.98.